EFFECTS OF TEMPERATURE ON METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR CHARACTERISTICS

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A thesis submitted in partial fulfillment of the requirements for Degree of the Master of Science of the Department of Physics, University of Eldoret

NOVEMBER, 2013

DECLARATION

Declaration by Candidate

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Declaration by Supervisors

This thesis has been submitted for examination with our approval as University supervisors.

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Moi University, Eldoret

2). Dr. David Waswa...……………………………..Date…………...……….

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DEDICATION

To my wife Edna and son Sammy

ABSTRACT

The metal-oxide-semiconductor field-effect transistor (MOSFET) is a transistor used for amplifying and switching on circuits. In this study, the MOSFET parameters were computationally modeled, analysed and presented. The study focused on the temperature parameter. The microscopic variations in structure are due simply to the probabilistic nature of device geometry and atomic processes hence require statistical predictions. In this work, a 30*nm* process was modeled and I-V curves and thermal analysis were modeled mathematically. The junction temperature depends on the thermal resistance and the temperature coefficient of threshold voltage reduced with increasing gate length. Further still the threshold voltage increased with doping concentration. Carrier mobility exhibited a strong and a complex dependence on temperature; it reduces with increasing temperature. Scattering mechanisms are temperature dependent. The sheet resistance increases with increasing temperature. This had a significant impact on the carrier mobility. The carrier mobility is shown not to vary with thickness. The MOSFET frequency response was found to degrade with increasing temperature. At high temperature; the threshold voltage, charge mobility, source voltage degrade. This consequently reduces the efficiency of the MOSFET devices. The study therefore obtained a balance between scaling down devices and it efficiency consequences. The cost of silicon is high and therefore being able to fabricate many devices on tiny wafer without compromising the speed is important. The study shows that a compromise between size and heat generation has to be found.

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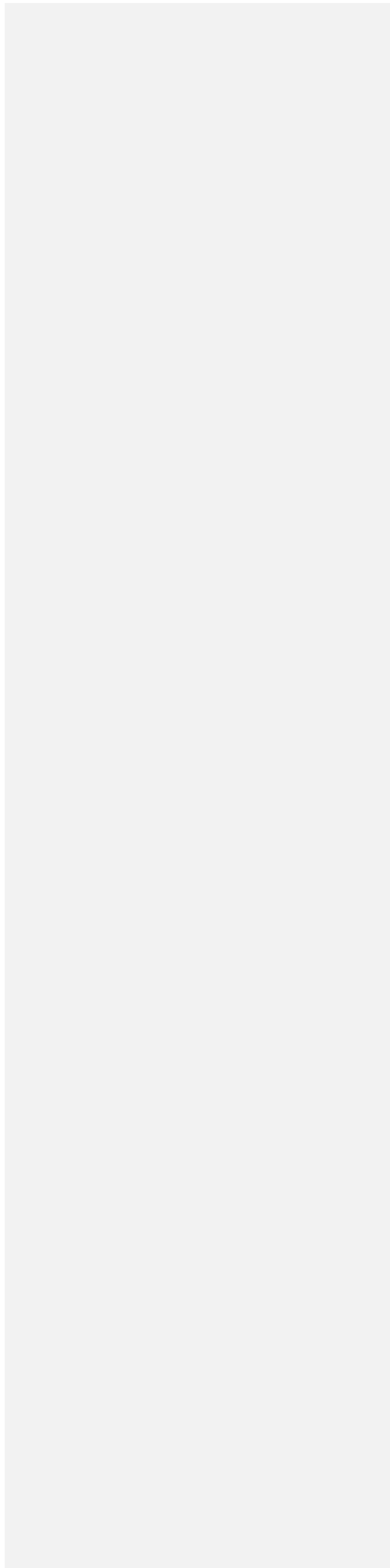

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SYMBOLS

E_g	Band gap Energy
$E_g(T)$	Bandgap energy as a function of temperature.
g_m	Transconductance
T	Temperature
,	Fitting parameters.
V_{GS}	Gate source Voltage
V_T	Device Voltage
V_{Th}	Threshold Voltage
V_{the}	Thermal voltage
V_{DS}	Drain Source Voltage
V_{Dsat}	Drain saturation voltage
V_{ov}	Overdrive Voltage.
C_{ox}	Oxide capacitance
C_D	Depletion Layer capacitance
K	Boltzmann Constant
n	Slope factor
W	Channel/gate width
L	Channel/Gate length
R_{ch}	Channel resistance

R_s , R_d	Series resistance.(source, drain)
R_{sh}	Sheet resistance
R_{sp}	Spreading resistances
R_{co}	Constant resistances
S	Distance between contacts via channel region
P_s	Sheet resistance per square
P_c	Interfacial specific constancy resistivity
N_s	Surface Impurity concentrations
	Potential barrier height
l_c	Minimum size
d	Spacing
t_{ac}	Surface accumulation layer thickness
R	Resistances
	Fit parameter to fit noise measurements
A	Pn junction area
q	Electric charge
	Proportionality constant
$Ø_f$	Surface potential

ABBREVIATIONS

IGFET	Insulated Gate Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect transistor
BSIM	Berkeley Short Channel IGFET Model
BJT	Bipolar Junction Transistor
MISFET	Metal insulator semiconductor Field effect transistor
IC	Integrated Circuit
SOI	silicon-on-insulator
IRTS	International Technology Roadmap for semiconductors
CMOS	Complementary Metal Oxide semiconductor
IBM	International Business Machines
JFET	Junction Field effect Transistor
FET	Field Effect Transistor

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CHAPTER ONE

INTRODUCTION

1.1 Introduction

This work focuses on the temperature effects on MOSFET parameters. Before that, an in-depth study, an overview of MOSFETs is made; the transformation over time it has undergone, the technicalities in design and use of MOSFETs. MOSFET structure and operations are highlighted. A brief look at fabrication and design techniques will be presented. Finally, the statement of the problem, objectives and justification of this work is stated. In all these, work towards achieving even higher merits for MOSFETs will be presented.

1.2 Historical background and recent development of MOSFETs

In 1959, Dawon Kahng and Martin Atalla at Bell Laboratories invented the metaló oxideósemiconductor field-effect transistor (MOSFET) as an offshoot to the patented Field-effect-transistor (FET) (Dawon and Martin, 2012) which is structurally and operationally different from the bipolar junction transistor. The MOSFET was made by introducing an insulating layer on the surface of the semiconductor and then placing a metallic gate electrode on it. It used crystalline silicon for the semiconductor and a thermally oxidized layer of silicon dioxide for the insulator. The silicon MOSFET did not generate localized electron traps at the interface between the silicon and its native oxide layer, and thus was inherently free from the trapping and scattering of carriers that had impeded the performance of earlier field-effect transistors. Following the development of clean rooms to reduce contamination to levels never before thought necessary, and of photolithography (Andrus, 1964), and the planar process to allow circuits to be made in very few steps, the SióSiO_2 system possessed such technical attractions as low cost of production (on a per circuit basis) and ease of integration. Additionally, the method of coupling two complementary MOSFETs (P-channel and N-channel) into one high/low switch, known as complementary metal oxide semiconductor (CMOS), meant that digital circuits dissipate very little power except when actually switched on. Largely because of these

three factors, the MOSFET has become the most widely used type of transistor in integrated circuit form. MOSFET transistors are the core of todayøs integrated circuits (ICs). Originally computers used mechanical switches to solve Boolean operations. But MOSFET transistors allowed computers to evolve and impact lives.

The two major types of transistors are the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and the Bipolar Junction Transistor (BJT). Digital integrated circuits almost exclusively use the MOSFET while the BJT has application in analog electronics. Transistors differ from passive resistors, capacitors, inductors, and diode devices because MOSFET transistor output current and voltage characteristics vary with the voltage on a control terminal. Transistors have three terminals concerned with signal transmission while passive devices have two terminals.

MOSFET fall under Field Effect Transistor (FET) together with Junction Field Effect (JFET). There are two types of MOSFET transistors, nMOS and pMOS that differ in the polarity of carriers responsible for transistor current. The charge carriers are holes in pMOS transistors and electrons in nMOS transistors.

1.3 Physical Structure of MOSFET

The MOSFET transistor construction begins with a lightly doped host crystalline substrate structure. nMOS substrate is doped with p-doped silicon, while the pMOS substrate use n-doped silicon. Figure 3.1 shows the transistor thin oxide (t_{ox}) thickness that electrically isolates the gate terminal from the semiconductor crystalline structures underneath. The gate oxide is made of oxidized silicon forming a non-crystalline, amorphous SiO_2. The gate oxide thickness (t_{ox}) typically ranges from near 1.5 nm. SiO_2 molecules are about 3.2Å in diameter so that this vital dimension is now a few molecular layers thick. The purpose of the SiO_2 dielectric is to allow an electric field generated by the gate voltage to influence the amount of charge passing between the drain and source. A thinner gate oxide allows the electric field gate to better control the device state and allows faster transistors. The thin gate oxide has sometimes been referred to as the beating heart of the transistor.

1.4 MOSFET scaling

Over the past decades, the MOSFET has continually been scaled down in size; typical MOSFET channel lengths were once several micrometres, but modern integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometers.. Historically, the difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process, the need to use very low voltages, and with poorer electrical performance necessitating circuit redesign and innovation (Dennards, 2013).

1.4.1 Reasons for MOSFET scaling

Smaller MOSFETs are desirable for several reasons. The main reason to make transistors smaller is to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, reducing the price per chip. In fact, over the past 30 years the number of transistors per chip has been doubled every 2ó3 years once a new technology node is introduced. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology can well be twice as many as in a 65 nm one. This doubling of transistor density was first observed by Gordon Moore in 1965 and is commonly referred to as Moore's law (Moore, 1965).

1.4.2 Trends in Transistor Gate Length

It is also expected that smaller transistors switch faster due to short channel length. For example, one approach to size reduction is a scaling of the MOSFET that requires all device dimensions to reduce proportionally. The main device dimensions are the transistor length, width, and the oxide thickness, each scale with a factor of 0.7 per node. This way, the transistor channel resistance does not change with scaling, while gate capacitance is cut by a factor of 0.7. Hence, the resistive capacitive (RC) delay of the transistor scales with a factor of 0.7.

While this has been traditionally the case for the older technologies, for the state-of-the-art, MOSFETs reduction of the transistor dimensions does not necessarily translate to higher chip speed because the delay due to interconnections is more significant.

1.5 Difficulties arising due to MOSFET size reduction

The study lists some of the major limiting factors that arise from the reduction of the MOSFET size.

1.5.1 Higher subthreshold conduction

As MOSFET geometries shrink, the voltage that can be applied to the gate must be reduced to maintain reliability. To maintain performance, the threshold voltage of the MOSFET has to be reduced as well. As threshold voltage is reduced, the transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available; the circuit design is a compromise between strong current in the ON case and low current in the OFF case, and the application determines whether to favor one over the other. Subthreshold leakage (including subthreshold conduction, gate-oxide leakage and reverse-biased junction leakage), which was ignored in the past, now can consume upwards of half of the total power consumption of modern high-performance VLSI chips. (Kaushik and Riat, 2004; Dragica *et al*, 2006)

1.5.2 Increased gate-oxide Leakage

The gate oxide, which serves as insulator between the gate and channel, should be made as thin as possible to increase the channel conductivity and performance when the transistor is ON and to reduce subthreshold leakage when the transistor is OFF. However, with gate oxides with a thickness of around 1.2 nm, the quantum mechanical phenomenon of electron tunneling occurs between the gate and channel, leading to increased power consumption (Dragica *et al*, 2006) Silicon dioxide has traditionally been used as the gate insulator but it has a modest dielectric constant. Increasing the dielectric constant of the gate dielectric allows a thicker layer while maintaining a high capacitance. All else equal, a higher dielectric thickness reduces

the quantum tunneling current through the dielectric between the gate and the channel.

Insulators that have a larger dielectric constant than silicon dioxide are being used to reduce the gate leakage from the 45 nm technology node onwards. On the other hand, the barrier height of the new gate insulator is an important consideration; the difference in conduction band energy between the semiconductor and the dielectric also affects leakage current level. For the traditional gate oxide, silicon dioxide, the forms barrier of approximately 8 eV. For many alternative dielectrics the value is significantly lower, tending to increase the tunneling current, somewhat negating the advantage of higher dielectric constant. (Kaushik and Riat, 2004; Dragica *et al*, 2006)

1.5.3 Increased Junction Leakage.

To make devices smaller, junction design has become more complex, leading to higher doping levels, shallower junctions, "halo" doping and so forth, (Wai-Kai, 2006) all to decrease drain-induced barrier lowering. To keep these complex junctions in place, the annealing steps formerly used to remove damage and electrically active defects must be curtailed increasing junction leakage. Heavier doping is also associated with thinner depletion layers and more recombination centers that result in increased leakage current, even without lattice damage.

1.5.4 Low Output Resistance

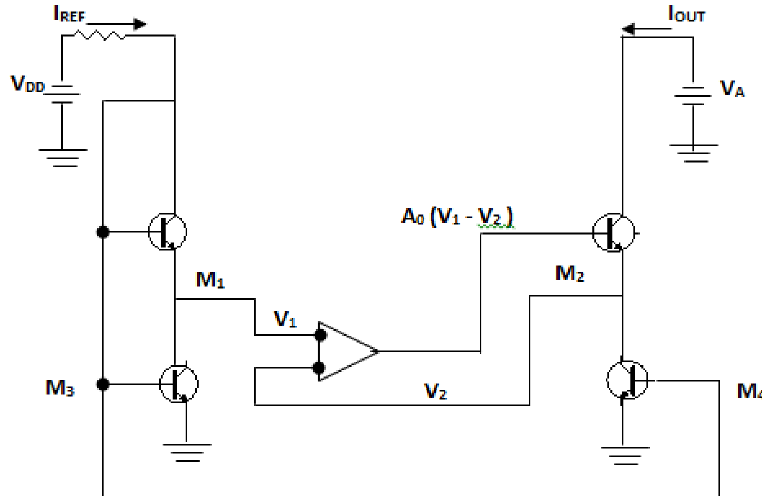


Fig. 1.1: BJT version of gain-boosted current mirror

For analog operation, good gain requires high MOSFET output impedance, which is to say, the MOSFET current should vary only slightly with the applied drain-to-source voltage. As devices are made smaller, the influence of the drain competes more successfully with that of the gate due to the growing proximity of these two electrodes, increasing the sensitivity of the MOSFET current to the drain voltage. To counteract the resulting decrease in output resistance, circuits are made more complex, either by requiring more devices, for example the cascade and cascade amplifiers, or by feedback circuitry using operational amplifiers, for example a circuit like that in the Figure 1.1 above. M1 and M2 are in active mode, while M3 and M4 are in Ohmic mode, and act like resistors. The operational amplifier provides feedback that maintains a high output resistance (Horowitz and Hill, 2011)

1.5.5 Lower Transconductance

The transconductance of the MOSFET determines its gain and is proportional to carrier mobility. As MOSFET size is reduces, the fields and dopant impurity in the channel increase. Both changes reduce the carrier mobility, and hence the transconductance. As channel lengths reduces without proportional reduction in drain

voltage, raising the electric field in the channel, the result is velocity saturation of the carriers, limiting the current and the transconductance (Arora, 2007).

1.5.6 Interconnect Capacitance

Traditionally, switching time was roughly proportional to the capacitance of gates. However, with transistors becoming smaller and more transistors being placed on the chip, interconnect capacitance (the capacitance of the metal-layer connections between different parts of the chip) is becoming a large percentage of capacitance (Soudris *et al*, 2000). Signals have to travel through the interconnect, which leads to increased delay and lower performance.

1.5.7 Heat Production

Fig. 1.2: Large heat sinks to cool power transistors in a TRM-800 audio amplifier (Soudris et al, 2000)

The ever-increasing density of MOSFETs on an integrated circuit creates problems of substantial localized heat generation that can impair circuit operation. Circuits operate more slowly at high temperatures, and have reduced reliability and shorter lifetimes. Heat sinks and other cooling devices and methods are now required for many integrated circuits including microprocessors.

Power MOSFETs are at risk of thermal runaway. As the ON-state resistance rises with temperature, then the power loss rises correspondingly, generating further heat. When the heat sink is not able to keep the temperature low enough, the junction

temperature may rise quickly and uncontrollably, resulting in destruction of the device.

1.5.8 Process Variations

With MOSFETs becoming smaller, the number of atoms in the silicon that produce many of the transistor's properties become less, with the result that control of dopant numbers and placement is more erratic. During chip manufacturing, random process variations affect all transistor dimensions: length, width, junction depths, oxide thickness *etc.*, and become a greater percentage of overall transistor size as the transistor shrinks. The transistor characteristics become less certain, more statistical. The random nature of manufacture means we do not know which particular example MOSFETs actually will end up in a particular instance of the circuit. This uncertainty forces a less optimal design because the design must work for a great variety of possible component MOSFETs (Michael *et al*, 2007)

1.5.9 Modeling Challenges

Modern ICs are computer-designed with the goal of obtaining working circuits from the very first manufactured lot. As devices are miniaturized, the complexity of the processing makes it difficult to predict exactly what the final devices look like, and modeling of physical processes becomes more challenging as well. These factors combine to make adequate simulation and manufacture difficult (Michael *et al*, 2007).

1.6 Uses of MOSFET

The n-channel enhancement mode MOSFET operates using a positive input voltage and has an extremely high input resistance (almost infinite) making it possible to interface with nearly any logic gate or driver capable of producing a positive output. Also due to this very high input (gate) resistance, many different MOSFETs can be parallel until the current handling limit required is achieved. Although there are various applications of MOSFETs in this work a brief look at the MOSFET as a switch is studied. While connecting together various MOSFETs may enable us to switch high currents or high voltage loads, doing so becomes expensive and

impractical in both components and circuit board space. To overcome this problem power field effect transistors (FETs) where developed.

By applying a suitable drive voltage to the gate of a FET the resistance of the drain-source channel can be varied from an off-resistance of many hundreds of kilo ohms, effectively a short circuit. The MOSFET can be turned on fast or slowly to pass high currents or low currents. This ability to turn the power MOSFET ON and OFF allows the device to be used as a very efficient switch with switching speeds much higher than standard bipolar junction transistors.

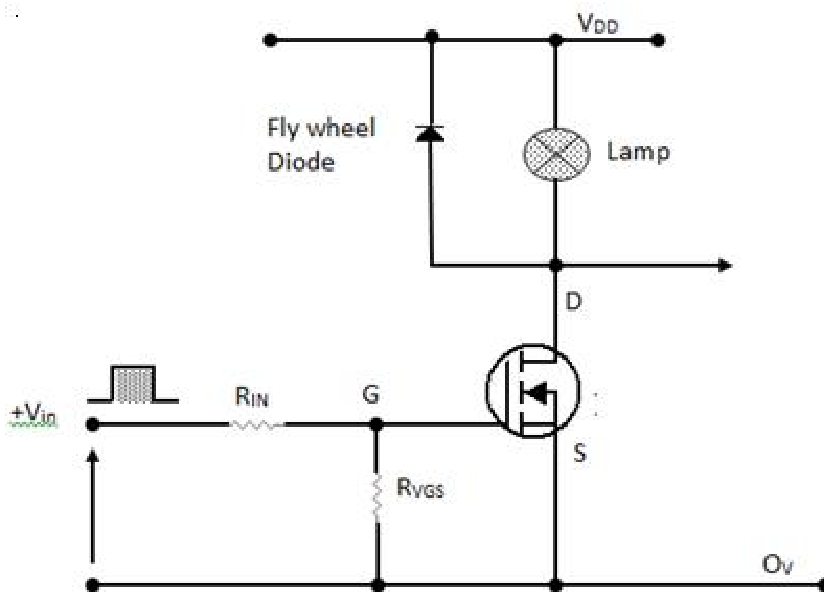


Fig. 1.3: An enhancement mode n-channel MOSFET used to switch a simple lamp
(Wayne, 2013)

In this circuit arrangement an enhancement-mode n-channel MOSFET is being used to switch a simple lamp ON and OFF. The gate input voltage V_{GS} is taken to an appropriate positive voltage level to turn the device and the lamp either fully ON (V_{GS} = +ve) or a zero voltage level to turn the device fully OFF (V_{GS}=0).

If the resistive load of the lamp was to be replaced by an inductive load such as a coil or solenoid, a ÷fly wheelø diode would be required in parallel with the load to protect the MOSFET from any back e.m.f.

For the power MOSFET to operate on analogue switching device, it needs to be switched between its ÷cut off regionø where V_{GS}=0 and its ÷saturation regionø where V_{GS}(ON)=+ve. The power dissipated in the MOSFET depends upon the current flowing through the channel I_D at saturation and also the ON-resistance of the channel given as R_{DS}(ON) (Wayne, 2013).

For example, assuming that the lamp is rated at 6 V, 24 W and is fully ÷ONø and the standard MOSFET has a channel õON-resistanceö (R_{DSO}) value of 0.1 ohms, on calculating the power dissipated in the MOSFET switch the current flowing through the lamp is calculated as

$P = VxI$, therefore $I_D = \frac{P}{V} = 24/6 = 4\text{Amps}$

Then the power dissipated in the MOSFET will be given as:

$P_D = I_D^2 x R_{DS}$, therefore, P_D=4^2x0.1=1.6 Watts.

(R_{DSO}) is ON channel resistance.

At high (R_{DSO}) channel resistance value would simply result in large amounts of power being dissipated within the MOSFET itself resulting in an excessive temperature rise, and which in turn could result in the MOSFET becoming very hot and damaged due to a thermal overload. But a low (R_{DSO}) value on the other hand is also desirable to help reduce the effective saturation voltage ($V_{DS(Sat)}$ = I_Dx(R_{DSO}) across the MOSFET. When using MOSFETs as a switch device, it is always advisable to select those that have very low (R_{DSO}) value or at least mount them onto a suitable heat sink to help reduce any thermal runaway and damage.

1.7 Statement of the Problem

Various researches have been done and findings reported on several other processes such as 150 nm, 90 nm amongst others (Nitin and Julka, 2011). With increasing demand for highly mobile and light electronic materials and considering that more than 99% of all ICs are MOSFETs, and that 10^6 MOSFETs per person per year are manufactured (Schubert, 2003). There is compelling need to reduce cost on raw materials and to scale down MOSFET devices and deal with the temperature effects as size reduces.

In order for this to be achieved, the size of the MOSFET device has to be reduced as is currently the basis of research, and effort to scale down the size to less than 30 nm process. This will deliberately affect MOSFET heat influenced parameters; like threshold voltage, frequency response, effective charge mobility, gate oxide to substrate capacitances, channel length and level of doping concentration. This in effect must either reduce the device performance. In this work, a simulation of the effect of temperature variations on MOSFET characteristics is performed.

1.8 Research Objectives

The following were the objectives of this study.

(i) To simulate the temperature effects on velocity saturation, resistances, mobility, drain currents at the 30nm process.
(ii) To study the effect of downscaling on MOSFET parameters

1.9 Significance of the study

The findings from this research will be used in the electronics industry. Kenya is setting up a hub city that is expected to spur development in the area of electronics. It is expected that the devices (MOSFET) study, science and technology will find extensive use in electronics.The areas of interest include semiconductor application technology, optic fibre and broadband etc. The study of MOSFETs will be vital in establishment of manpower capable of carrying out research and development in this field. In being part of this wide challenge, the research is determined to have an in depth study of the aforementioned properties of MOSFET.

CHAPTER TWO

LITERATURE REVIEW

2.1 Introduction

This chapter reviews the effort and work done so far on MOSFETs especially on the temperature parameter effects. A lot of work has been done on MOSFET both in the theoretical simulations and experiments with studies in parameters like gate length, gate source current, impurities presence, ion implication effects on fabrication techniques, and structural characteristics among many other features.

2.2 MOSFETs

The metal-oxide-semiconductor field effect transistor (MOSFET) is a transistor used for amplifying or switching electronic signals (Gray *et al*, 2001). In MOSFETs, a voltage on the oxide-insulated gate electrode can induce a conducting channel between the two other contacts called source and drain. The channel can be of n-type or p-type and is accordingly called nMOSFET or a pMOSFET (also commonly known as nMOS, pMOS). It is by far the most common transistor in both digital and analog circuits, though the bipolar junction transistor was at one time much more common (Ytterdal *et al*, 2003; Sze and Kwok, 2006)

Usually the semiconductor of choice is silicon, but some chip manufacturers, most notably IBM and INTEL, recently started using a chemical compound of silicon and germanium (SiGe) in MOSFET channels. Unfortunately, many semiconductors with better electrical properties than silicon, such as gallium arsenide, do not form good semiconductor-to-insulator interfaces, thus are not suitable for MOSFETS. In order to overcome the increase in power consumption due to gate current leakage, a high-k dielectric is used instead of silicon dioxide for the gate insulator while polysilicon is replaced by metal gates. Van de Mer reports that channel leakage currents consist of drain-source currents, which are present even when gate-source voltage is zero (Van. der mer, 2004). There are three effects contributing to channel leakage currents namely:

i. Weak inversion current.
ii. Drain-induced barrier lowering (DIBL) current
iii. Channel edge current (Van. der mer, 2004)

The report states that weak inversion current, sometimes called subthreshold leakage when the transistor is used as a turned-off-switch. Their drain current relations in weak inversions are:

$$I_D = I_{DO} \exp(\frac{V_{GS} - V_{th}}{nV_T}) \quad 2.1$$

Some micro power analog circuits are designed to take advantage of subthreshold conduction. By working in the weak inversion region, the MOSFETs in these circuits deliver the highest possible transconductance-to-current ratio. (Eric, 1996; Masfred *et al.*, 2002; Satish, 2004).

The subthreshold I-V curve depend exponentially upon threshold voltage, introducing a strong dependence on any manufacturing variation that affects threshold voltage, for example, variations in oxide thickness, junction depth, or body doping that change the degree of drain-induced barrier lowering. The resulting sensitivity to fabrication variations complicates optimization for leakage and performance (Sandeep *et al*, 2004; Ashish *et al*, 2005)

In circuitry, the MOSFET is used in a digital, complementary metal-oxide-semiconductor (CMOS) logic which uses p and n-channel MOSFETS as building blocks. Overheating is reported as a major concern in integrated circuits since even more transistors are packed into even smaller chips (Wanlass, 2012). It is further demonstrated in the Fairchild R & D laboratory that logic circuits combining p-channel and n-channel MOS transistors in a complimentary symmetry circuit configuration draw close to zero power in a standby mode (Wanlass, 2012)

2.3 Operation Parameters

It is a well-known fact that the change in operation temperature of a device will influence its characteristics and hence the circuit performance. In a MOSFET model, there are many temperature dependent parameters such as (Yuhna *et al*, 1997)

i. mobility
ii. threshold voltage
iii. saturation velocity
iv. series parasitic resistances

Nitin and Julka, reported temperature fluctuation induced variations in individual device parameters have unique effects on MOSFET drain current (Nitin and Julka,2011). Device parameters that characterize the variations in MOSFET current due to temperature fluctuations are identified for 180 nm and 65 nm CMOS technologies. Operating an integrated circuit at the prescribed nominal supply voltage is not preferable for reliable circuit operation under temperature variations. Circuits display a temperature variation insensitive behaviour when operated at a supply voltage 45 % to 53 % lower than the nominal supply voltage for circuits in a 180 nm CMOS technology. Similarly, the optimum supply voltages are 68 % to 69 % lower than the nominal supply for circuits in a 65 nm CMOS technology.

Critical charge variation is caused by gate length and threshold voltage variations. For memory elements, if a charge deposited by the particle strike at the storage node is more than a minimum value, the node will be flipped and a soft error occurs. This minimum value is called critical charge. The critical charge is used by many researchers to measure the circuitøs vulnerability to soft errors (Animesh, 2008)

Process and environmental parameter variations in CMOS technologies are posing greater challenges in the design of high performance integrated circuits (John, 2004).

Performance of an integrated circuit under temperature fluctuations is determined by a set of device parameters. Temperature fluctuations alter threshold voltage, carrier mobility, and saturation velocity of a MOSFET (Cheng *et al*, 1999). At higher supply voltages, the drain saturation current of a MOSFET degrades when the temperature is increased. Alternatively, provided that the supply voltage is low, MOSFET drain

current increase with temperature, indicating a change in the dominant device parameter (Nitin and Julka, 2011).

The effect of velocity saturation on transistorøs internal characteristics and external factors has been widely discussed. Velocity saturation is caused by the increased scattering rate of energetic electrons, particularly optical phonon emission resulting in the degrading effect of the carrier mobility. Velocity saturation becomes more pronounced in short channel devices as they operate at high electric field. It yields smaller drain saturation currents and voltage values than that predicted by the ideal long channel relation. It is reported that surface-roughness scattering within the inversion layer is a function of the effective field independent of the doping concentration (Tan *et al*, 2006).

Deep-submicron CMOS technologies operating with low voltages and short gate lengths will be required for ICs which combine very high levels of interaction and low power (Saavedra, 1997). Saavedra also demonstrated a linear region fits for a set of successively reducing channel lengths. The linear region for low V_{GS} get slightly worse as the channel length decreases. It is suspected that this degradation is caused by an unwanted compiling of the linear and subthreshold parameters.

Berkeley short-channel insulated gate field effect transistors (IGFET) model (BSIM3v3) was developed to achieve robustness, accuracy and scalability for circuit simulation (Cheng, 1995). Additionally reported much work being done to model the inversion layer mobility for a wide range of channel doping concentration, gate and substrate voltages, as well as temperature. It is well known that phonon scattering, surface scattering and coulomb scattering are the three major scattering mechanisms governing the characteristic of carrier mobility in the inversion layer with phonon scattering being the dominant mechanisms at higher temperature(Cheng, 1996).

(Yuhna *et al*, 1997), modeled transconductance (g_m) and drain source transconductance (g_{ds}) with the temperature dependences of mobility, threshold voltage, saturation velocity and series resistance. The threshold voltage is a parameter that is sensitive to temperature change. It increases as temperature decreases due to Fermi level and band gap energy shifts. Threshold voltage also depends linearly on

the temperature over a wide range of temperature for the devices with a longer channel length.

MOSFETs fabrication on Silicon On Insulator substrates by applying novel schottky barrier height modulation technique of Erbium(Er) was reported by Hosoda and co-workers (Hosoda *et al*, 2008). Schottky barrier source/drain MOSFET (SB-MOSFET) is one of the promising inventions for the next generation of highly miniatured CMOS devices, thanks to its shallow junction depth with low sheet resistance and lower process temperature (Zhu and Gildenbat, 2011; Jun *et al*, 2008)). However, high schottky barrier height (ϕ_B) decreases the drive current of SB-MOSFETs). Erbium silicide has been proposed for n-channel SB-MOSFETs (SB-nMOSFETs) because of very low ϕ_B of 0.27-0.36 eV for electrons (Tan *et al*, 2006).

In vivo measurements of applied dose during radiotherapy treatment, it is important to ensure accurate dose delivery is done to patients (Tsang *et al*, 2004). A MOSFET device has the feature of integrating dose measurements as well as achieving immediate dose read out (Thomson and Thomson, 1984). Combining this with a very small sensing volume provides many advantages for a MOSFET dosimetry system in radiotherapy. As such MOSFET detectors are finding applications in radiotherapy dosimetry (Rosenfeld, 2002; Rozenfeld, 1996). A MOSFET domestic ability relies on the measurements of its threshold voltage (Rosenberg, 1995). By applying a significant large voltage to the MOSFETøs silicon gate, a significant number of holes will be attracted to the oxide/silicon surface from the silicon substrate as well as the source and drain regions. When a sufficient concentration of holes has accumulated, a conduction channel is formed, allowing current to flow between the source and drain. The voltage necessary to initiate current flow is known as the threshold voltage (Rossenfeld *et al*, 2001). When a MOSFET device is irradiated, three things occur within the detectors active volume: (i) a buildup of trapped charge in the oxide, (ii) an increase in the number of interface traps and (iii) an increase in the number of bulk oxide traps. These physical characteristics produce a change in the devices threshold voltage and as such, a measurement for absorbed dose can be performed by comparison of threshold voltages before and after irradiation. To be performed with a high degree of accuracy, the time of measurement before and after irradiation should

be kept constant. One limiting factor in the use of MOSFETs in vivo dosimetry is the inherent thermal errors intrinsic to MOSFET devices (Savic, 1995; Rosenberg, 1995).

The transistor density on a CMOS chip doubles approximately after every one and a half years (Schaller, 1997; Moore, 1998). Continuing with the Mooreø law, the gate length of the MOSFET will eventually shrink to 10nm by 2015. The reduced dimensions of the device mostly affect the mobility in the inversion layer of the MOSFET. But as we scale down the MOSFET, carrier mobility decreases due to the high vertical electrical fields in the substrate. The reduction in carrier mobility is a major cause of drain current degradation. This reduces the speed of the device.

2.4 Empirical Mobility Models

Several empirical models for the carrier mobility in the inversion layers of MOSFET, as a function of electric field have been reported (Mansour *et al*, 1972, Coughey and Tthomas, 1967). The measured effective mobility of electrons in the inverted <100> Si surface over a wide range of temperatures, gate voltages and back-bias voltages is calculated experimentally as a function of effective electric field at the doping concentration of $2.31 \times 10^{15} cm^{-3}$ (Sabins, 1995).

In nanoscale devices the mobility of carriers can be increased by using the strained silicon technology. When oxide thickness is below approximately 10 nm, carrier mobility is degraded (Choi *et al,* 1995). To enhance the mobility in the inversion layer of MOSFETS, strained-Si is regarded as possible alternatives to conventional Si devices mostly for deep submicron devices.

The electron mobility and concentration in double-gate silicon-on-insulator (SOI) gate-all around transistors is extracted by Hall effect measurements at room and liquid nitrogen temperature is reported (Vandooren *et al*, 2001). The hall mobility is compared with the drift mobility determined from the transconductance measurement of the devices in strong inversion. The experiment reveals high carrier mobility dominated at room temperature by phonon scattering mechanism and at low temperature by mixed scattering processes, with a predominance of the surface roughness scattering mechanism.

The operation of thin-film double-gate transistors is based on the concept of volume inversion (Balestra *et al*, 1987) according to which the minority carriers are no longer confined at the interfaces but spread out across the silicon film. In the centre of the film, far from the interfaces, carriers have presumably a higher mobility. Recent measurements on a 3-nm-thick SOI MOSFETs have shown a considerable gain in field-effect mobility for operation in double-gate mode as compared with single-gate mode (Ernst *et al*,1999).

MOSFETs suffer from many physical effects. To overcome these limitations solutions were proposed by different researchers. One of the proposed solutions was the use of high dielectric materials as gate insulator (Mudanai *et al*, 2000; Kawamoto and Janeson, 2000; Cheng *et al*, 1997).

MOSFET simulations and modeling has left its infancy and has reached a level whereby high agreement is reached with experimental characteristics (Simeon *et al*, 1996). At the same time, by building in temperature dependent physical models, it is possible to predict the low temperature operation in an accurate way (Selberherr, 1984; Selberherr, 1989). The Fowler and Hartstein (FH) method determines the point of maximum slope in the transconductance, g_m characteristic and linearly extrapolates this point to zero transconductance. Another technique introduced by Balestra and Ghibando is well suited for ceramic MOSFETs and is used to extract effective mobility (Hartstein, 1988). Probably the most powerful and fairly simple method for threshold voltage V extraction is the so-called transconductance peak or double derivative method which gives the dependence of saturation velocity on temperature inversion change and electric field in a nanoscale MOSFET. The intrinsic velocity is shown to be the ultimate unit to the saturation velocity in a very high electric field. The unidirectional intrinsic velocity arises from the fact the randomly oriented velocity vectors in zero electric field are streamlined and become unidirectional giving the ultimate drift velocity that is limited by the collision-free intrinsic velocity. In the non-degenerate regime, the intrinsic velocity is the thermal velocity that is a function of temperature and does not sensitively depend on the carrier concentration. In the degenerate regime, the intrinsic velocity is the Fermi velocity that is a function

of carrier concentration and independent of temperature. The presence of a quantum emission lowers the saturation velocity (Wong, 1987).

The lowest conduction sub-band energy verses position along the channel of a 10 nm MOSFET under a variety of gate and drain biases has been shown (Lundstrom, 2002). The results show that there is an energy barrier between the source and channel and that the height of the barrier is modulated by the gate voltage. The drain current increases as the barrier height reduce by the increasing gate voltage. For an electrostatically well designed MOSFET, the drain bias has a small effect on the height of the source to channel barrier. Lundstrom showed in their experimental results, that the parasitic bipolar transistor of the SOI-MOS structures behaves as ordinary bipolar device. Bipolar current gain increases with temperature causing premature breakdown and latch at elevated temperatures. This is because several physical constraints occur at these elevated temperatures.

At cryogenic temperatures hysteresis effects deteriorate the performance of PD SOI MOSFET devices. However twin-gate structure improves the cryogenic operation of PD SOI MOSFETs. For the twin gate structure in linear operation, the output curves show little hysteresis, while in saturation, some kink and hysteresis effect is still visible, although reduced compared with a single-gate transistor (Simeon *et al*, 1996).

2.5 Temperature Dependences

MOSFET characteristics are dependent on three temperatures, which represents the average kinetic energy of the three quasi-particle species: electrons, holes and phonons. The carriers, either electron or hole, with a carrier temperature several times higher than the lattice temperature are called hot carriers. This section describes the dependence of the transistor characteristics on the lattice temperature without considering the carrier temperature as being different from the lattice temperature. Such a treatment proves sufficiently accurate for the purpose of constructing a compact model for device simulation. Different from a metal, the number of carriers in a semiconductor increases as the temperature increases. However, the temperature dependence of the output characteristics are not that simple in real devices (Nitin and Julka, 2011, Sze and Kwok, 2006).

The energy bandgap of semiconductors tends to decrease as the temperature is increased. This behavior can be understood if one considers that the interatomic spacing increases when the amplitude of the atomic vibrations increases due to the increased thermal energy. This effect is quantified by the linear expansion coefficient of a material. An increased interatomic spacing decreases the average potential seen by the electrons in the material, which in turn reduces the size of the energy bandgap. A direct modulation of the interatomic distance such as by applying compressive (tensile) stress also causes an increase (decrease) of the bandgap.

The temperature dependence of the energy bandgap, E_g, has been experimentally determined yielding the following expression for E_g as a function of the temperature, T. (Sze and Kwok, 2006)

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \qquad 2.2$$

Where $E_g(0)$, and are the fitting parameters. These fitting parameters are listed for germanium, silicon and gallium arsenide in Table2:

Table 2.1: Fitting parameters for different elements.

	Germanium	Silicon	GaAs
$E_g(0)$ (eV)	0.7437	1.166	1.519
α (meV/K)	0.477	0.473	0.541
β (K)	235	636	204

Nitin, reports that temperature fluctuations alter threshold voltage, carrier mobility, and saturation velocity of a MOSFET (Nitin and Julka,2011). Temperature fluctuation induced variations in individual device parameters have unique effects on MOSFET drain current. They present an optimum supply voltage of 68 % and 69 % lower than the nominal supply voltage for circuits in a 65 nm CMOS technology (Sagura and Charles, 2004; Sze and Kwok, 2006).

CHAPTER THREE

THEORY

3.1 Introduction

An Insulated-Gate Field-Effect Transistor (IGFET) is a related term almost synonymous with MOSFET. The term may be more inclusive, since many "MOSFETs" use a gate that is not metal, and a gate insulator that is not oxide. Another synonym is MISFET for metalóinsulatorósemiconductor FET.

MOSFET transistors are the core of todayøs integrated circuits (ICs). Originally computers used mechanical switches to solve Boolean operations. The purpose is to acquire the analyticalability and transistor insights that engineers use to design and troubleshoot digital ICs.

3.2 MOSFET Structure

Figure 3.1 sketches a MOSFET transistor. The bottom rectangular block of material is the silicon substrate often referred to as the bulk. There are four electronically active regions that are marked gate (G), source (S), and drain (D), and the bulk terminal (B) to which the gate, drain, and source voltages are typically referenced. The rectangular gate region lies on top of the bulk separated by a thin silicon oxide dielectric with thickness T_{OX}. Two other important dimensions are the transistor gate length and width. The drain and source regions are embedded in the substrate but have an opposite doping to the substrate.

The nMOS transistor has a p-doped silicon substrate with n-doping for the drain and source. pMOS transistors have a complementary structure with an n-doped silicon bulk and p-doped drain and source regions. The gate region above the thin oxide dielectric is constructed with polysilicon in both transistors. Polysilicon is made of many small silicon crystals. The region between the drain and source just under the gate oxide is called the channel, and is where charge conduction takes place. The distinction between the two transistors is that electrons are the channel current in the nMOS transistor, and holes are the channel current in the pMOS transistor. Since

drain and source dopants are opposite to the substrate (bulk), they form pn junction diodes that are either reverse or zero biased in the substrate (bulk), as shown in fig. 3.2(a) and (b).

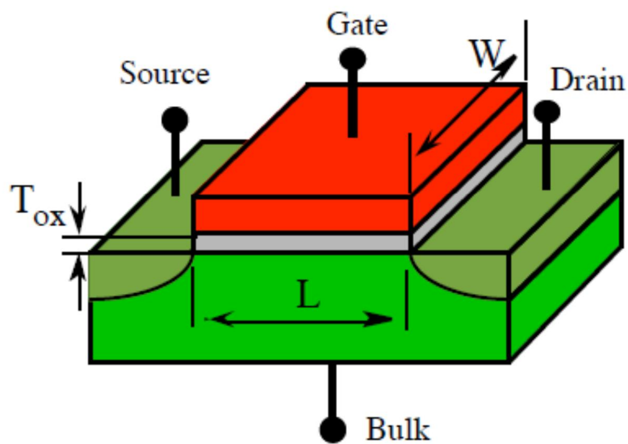
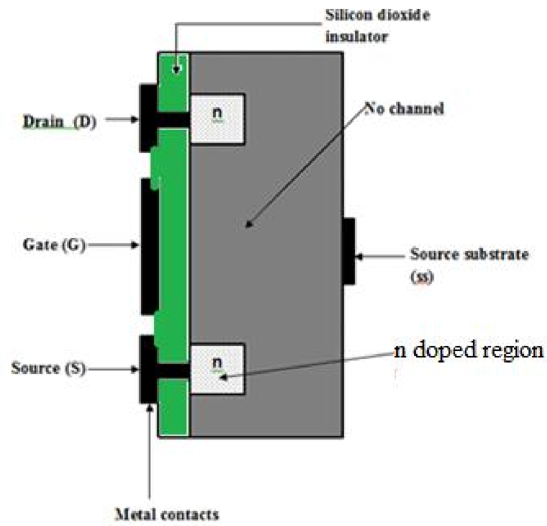
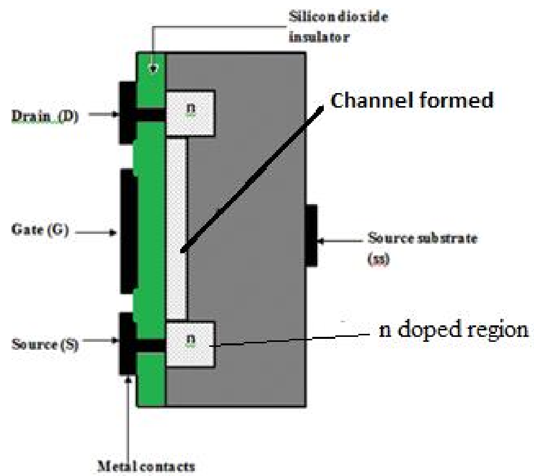


Figure 3.1: shows symbols commonly used for MOSFET (Hawkins et al, 2010)



(a)



(b)

Fig. 3.2: (a) Cross section of an NMOS without channel formed: OFF state and (b) NMOS with channel formed: ON state.

The distance from the drain to the source is a geometrical parameter called the channel length (L) and the lateral dimension is the transistor channel width (W) as is indicated in Figure 3.1. Transistor length and width are parameters set by the circuit designer and process engineer. The width to length ratio (W/L) is linearly related to the drain current capability of the transistor. A wider transistor will pass more current. The gate is the control terminal, while the source provides electron or hole charge carriers that empty into the channel and are collected by the drain.

Other parameters, such as the transistor oxide thickness, threshold voltage, and doping levels depend on the fabrication process and cannot be changed by design. These are technology parameters set by the process and device engineers.

3.3 MOS Transistor Operation: Descriptive Approach

Transistors must have exact terminal voltage polarities to operate as seen in Figure 3.3. The bulk or substrate of nMOS (pMOS) transistors must always be connected to the lower (higher) voltage that is the reference terminal. The bulk is usually connected to ground for an nMOSFET, and the bulk of a pMOSFET is connected to the power supply voltage. It is assumed that the bulk and source terminals are shorted in Si (pMOS) device. The current between drain and source is referred to as drain source current (I_{DS} or simply I_D). When a voltage is applied to the drain terminal, the drain current depends on the voltage applied to the gate control terminal. V_{GS}, V_{DS} and I_{DS} are negative values for pMOS transistors.

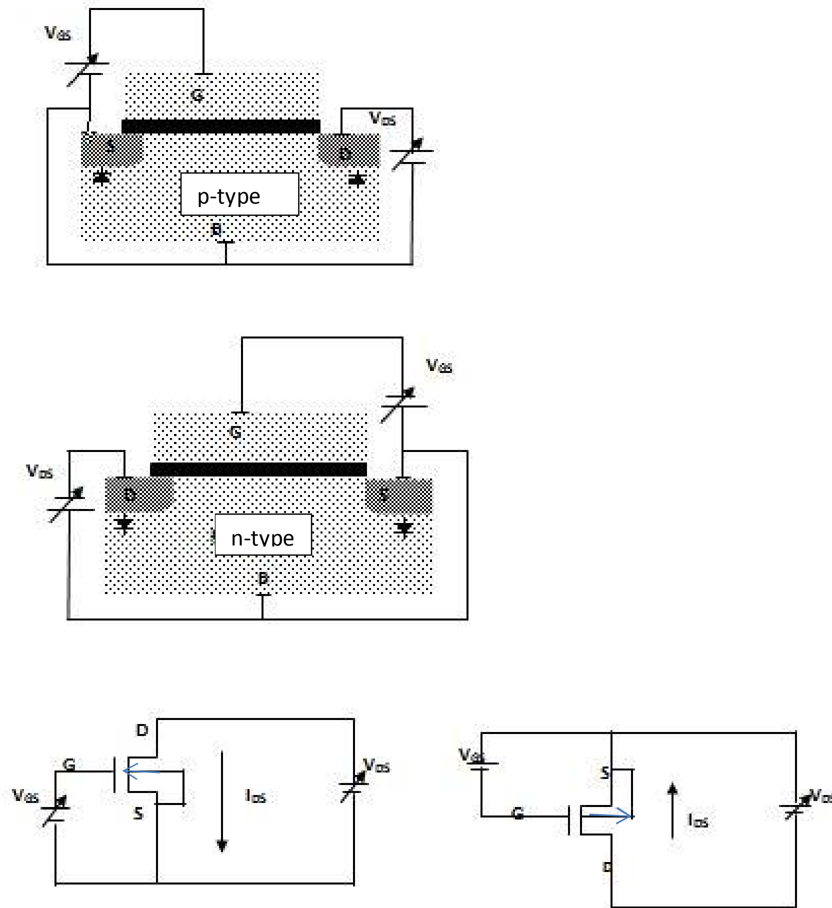
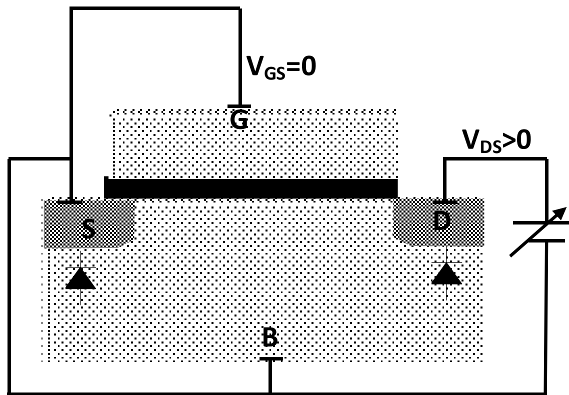
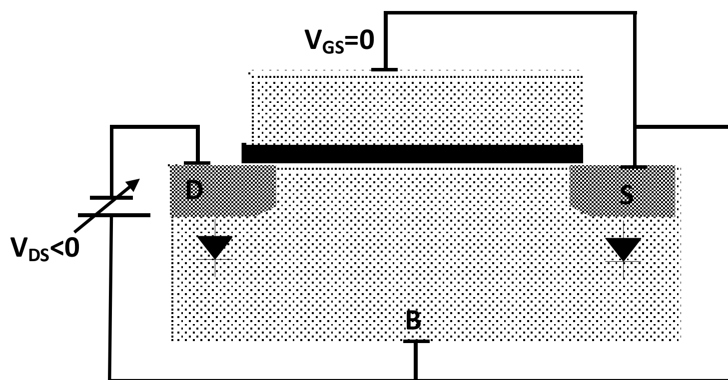


Fig.3.3: Transistor biasing for nMOS and pMOS structures

A channel of free carriers requires a minimum gate to source threshold voltage to induce a sheet of mobile charge. If V_{GS} is zero in an nMOS device, then there are no free charges between the drain and source and an applied drain voltage reverse-biases the drain-bulk diode as seen in Figure 3.4. This is the OFF or non-conducting state of the transistor.



(a)



(b)

Fig. 3.4: Transistor biasing with gate source voltage set to zero. (a) nMOS (b) pMOS

3.4 Modes of Operation

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals. In the following discussion, a simplified algebraic model is used that is accurate. Modern MOSFET characteristics require computer models that have rather more complex behaviour.

For an enhancement-mode, n-channel MOSFET, the three operational modes are:

(i) Cut-off,

(ii) subthreshold or linear mode

(iii) weak-inversion mode

When V_{GS}<V_{Th}, where V_{Th} is the threshold voltage of the device, according to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source. At this point, the MOSFET is said to be in cutoff mode. In reality, the Boltzmann distribution of electron energies allows some of the more energetic electrons at the source to enter the channel and flow to the drain, resulting in a subthreshold current that is an exponential function of gateósource voltage. While the current between drain and source should ideally be zero when the transistor is being used as a turned-off switch, there is a weak-inversion current, sometimes called subthreshold leakage.

In weak inversion the current varies exponentially with gate-to-source bias V_{GS} as given approximately by:

$$I_D = I_{DO} e^{(V_{GS} - V_{the}) / nV_T} \quad 3.1$$

where I_{D0} is current at $V_{GS} = V_{The}$, the thermal voltage $V_{The} = kT / q$ and the slope factor n is given by

$$n = 1 + \frac{C_D}{C_{OX}} \quad 3.2$$

with C_D = capacitance of the depletion layer and C_{OX} = capacitance of the oxide layer. In a long-channel device, there is no drain voltage dependence of the current once $V_{DS} >> V_T$, but as channel length is reduced drain-induced barrier lowering introduces drain voltage dependence that depends in a complex way upon the device geometry. Frequently, threshold voltage V_{Th} for this mode is defined as the gate voltage at which a selected value of current I_D occurs.

By working in the weak-inversion region, the MOSFETs in these circuits deliver the highest possible transconductance-to-current ratio; almost that of a bipolar transistor, namely:

$$\frac{g_m}{I_D} = \frac{1}{nV_T} \quad (3.3)$$

The subthreshold $I–V$ curve depends exponentially upon threshold voltage, introducing a strong dependence on any manufacturing variation that affects threshold voltage; for example: variations in oxide thickness, junction depth, or body doping that change the degree of drain-induced barrier lowering. The resulting sensitivity to fabrication variations complicates optimization for leakage and performance.

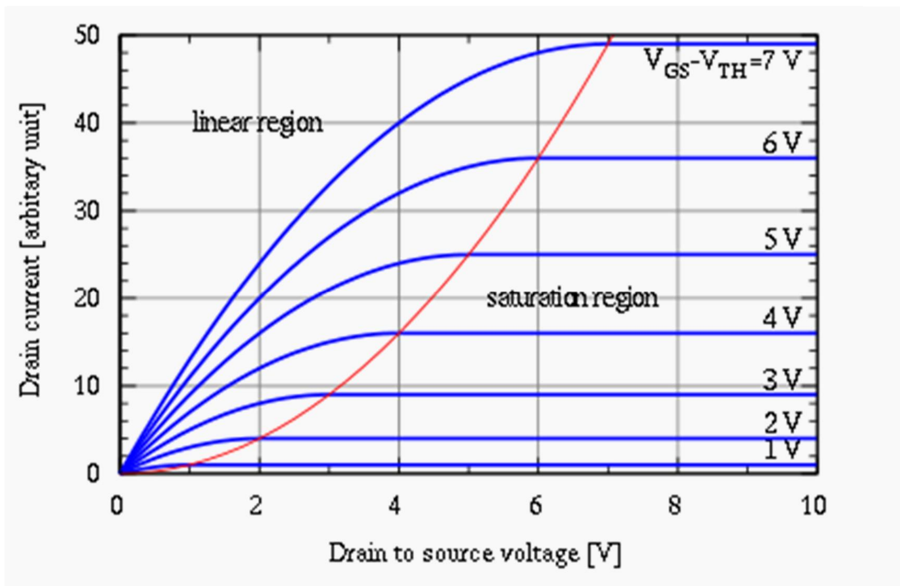


Fig. 3.5: MOSFET drain current vs. drain-to-source voltage (Galup-montoro and Schneider, 2007).

The boundary between linear (Ohmic) and saturation (active) modes is indicated by the upward curving parabola (Galup-montoro and Schneider, 2007).

3.4.1 Triode Mode or Linear Region (also known as the ohmic mode)

When V_{GS} >V_{th} and V_{DS} < (V_{GS} ó V_{th}), the transistor is turned ON, and a channel is created which allows current to flow between the drain and the source. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The current from drain to source is modeled as (Galup-montoro and Schneider, 2007).

$$I_D = \mu_n C_{ox} \frac{W}{L}\left(\left(V_{GS} - V_{th}\right)V_{DS} - \frac{V_{DS}^2}{2} \right) \qquad 3.4$$

Where $_n$ is the charge-carrier effective mobility, W is the gate width, L is the gate length and C_{ox} is the gate oxide capacitance per unit area. The transition from the exponential subthreshold region to the triode region is not as sharp as the equations suggest.

3.4.2 Saturation or Active Mode

When $V_{GS} > V_{Th}$ and $V_{DS} > (V_{GS} - V_{Th})$

The switch is turned ON, and a channel is created, which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage, the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as pinch-off to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gateósource voltage, and modeled approximately as (*Galup-montoro and Schneider, 2007*).

$$I_D = \frac{\mu_n C_{ox} W}{2L}\left(V_{GS} - V_{th}\right)^2 \left(1 + \lambda\left(V_{DS} - V_{DSat}\right)\right) \qquad 3.5$$

Where V_{Dsat} is the drain saturation voltage, the additional factor , is the channel-length modulation parameter. This equation models current dependence on drain

voltage. According to this equation, a key design parameter, the MOSFET transconductance is:

$$g_m = \frac{2I_D}{V_{GS} - V_{th}} = \frac{2I_D}{V_{ov}} \quad 3.6$$

Where the combination $V_{ov} = V_{GS} - V_{th}$ is called the overdrive voltage, and where $V_{DSsat} = V_{GS} - V_{th}$, which (Saavedra, 1997), neglects accounts for a small discontinuity in I_D which would otherwise appear at the transition between the triode and saturation regions.

Another key design parameter is the MOSFET output resistance r_{out} given by:

$$r_{out} = \frac{1}{\lambda I_D} \quad 3.7$$

If is taken as zero, an infinite output resistance of the device leads to unrealistic circuit predictions, particularly in analog circuits.

As the channel length becomes very short, Equations 3.5, 3.6, 3.7 become quite inaccurate as new physical effects arise. For example, carrier transport in the active mode may become limited by velocity saturation. When velocity saturation dominates, the saturation drain current is more nearly linear than quadratic in V_{GS}. At even shorter lengths, carriers transport with near zero scattering, known as quasi-ballistic transport results. In addition, the output current is affected by drain-induced barrier thus lowering the threshold voltage.

3.5 MOSFET Capacitances

The transient behavior of a MOSFET is due to the device capacitive effects which in fact are the results of the charges stored in the device. The stored charges are; the inversion charge q_i in the inversion or channel region, the bulk charge in the depletion region underlying the channel, the gate charge at the gate terminal and the charges due to the source/drain pn-junctions (Arora, 2007). These charges give rise to the device capacitances. From the point of developing MOSFET dynamic or transient

models, it is instructive to divide the device into two parts: the intrinsic part which forms the channel region of the device, and is mainly responsible for the transistor action. The charges which are responsible for the transistor action are the gate charge (q_g), the depletion or bulk charge (q_b) and the inversion charge (q_i). The capacitances arising from these charges are called intrinsic capacitances. Thus capacitances c_{gs}, c_{gd} and c_{ds}, shown in Figure 3.6, are the intrinsic capacitances. The simple first order MOSFET capacitance model assumes only these three intrinsic capacitance, but in fact there are many more.

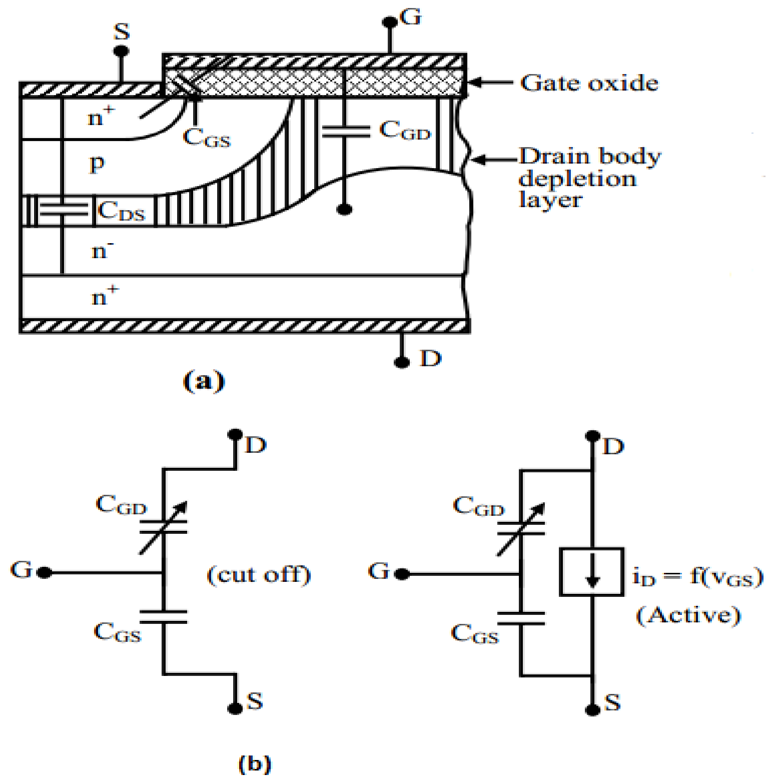


Fig. 3.6: (a) MOSFET capacitance and (b) circuit symbols (Kharagpur, 2010)

These intrinsic capacitances are normally derived from the charges which are used to calculate the steady-state current I_{DS}. Thus the capacitance expressions do not involve any new parameters other than those required for I_{DS} calculations.

3.5.1 MOSFET Parasitic Elements

The source/drain junction portion of a MOSFET is a parasitic component. These parasitic elements (resistance and capacitance) limit the drive capability and switching speed of the device and therefore should be minimized. However, source drain is an essential part of the device, therefore these effects cannot be eliminated. It is therefore important to model these elements in order to simulate the device switching behavior accurately.

It is important to note that for too long channel devices, the series resistance R_S and R_D are negligible compared to the channel resistance. The channel length resistance being directly proportional to channel length L, the higher the L, the higher the channel resistance. The channel resistance can be given by

$$R_{ch} = \frac{1}{g_{ds}} = (\frac{\partial I_{ds}}{\partial v_{ds}})^{-1} = \frac{L}{W} * \frac{1}{\mu COS(v_{gs} - v_{th} - v_{ds})} \quad \text{(Arora,2007)} \qquad 3.8$$

However, as the channel length L decreases the series resistance R_S and R_D become appreciable fractions of R_{ch} and thus can no longer be neglected.

The resistance R_s which is in series with the channel resistance R_{ch}, can be expressed as sum of three terms.

$$R_s = R_{sh} + R_{co} + R_{sp} \qquad 3.9$$

Where R_{sh} is the sheet resistance of the heavily doped source (drain) diffusion region where the current flows along the parallel lines, R_{CO} is the constant resistance between the metal and the source (drain) diffusion region, and R_{sp} is the spreading resistance due to the current lines crowding near the channel end of the source (drain).

The sheet resistance R_{sh} is simply given by

$$R_{sh} = \frac{P_s S}{W} \qquad 3.10$$

Where S is the distance between the contacts via the channel region P_s is the sheet resistance per square (R/square) and W is device width.

Within the contact area, the voltage drop in the diffused region results in current crowding near the front end of the contact. This effect results in a contact resistance R_{co}. For a rectangular contact of length l_c, then

$$R_{co} = \frac{\sqrt{P_c P_s}}{W} \coth\left(l_c \sqrt{\frac{P_s}{P_c}} \right) \text{ (Arora,2007)} \qquad 3.11$$

Where P_c is the interfacial specific contact resistivity (á /cm^2) between the metal and source (drain) region.

The magnitude of P_c depends on a charge transport mechanisms and is determined primarily by the surface impurity concentration N_s, potential barrier height ϕ and ambient temperature T. In practice P_c is sensitive to the metal-silicon interface preparation procedure. In particular, the presence of an oxide in the contact hole strongly affects P_c. Equation (3.11) assumes that all channel width is used for the contact. However, this is not generally the case and multiple standard contacts of minimum size l_c separated by spacing d are used therefore Equation (3.11) is multiplied by a factor $1 + \frac{d}{l_c}$

The sheet resistance Rs, is the spreading resistance R_{sp} which arise from the radial pattern of current spreading from the MOSFET channel, which has a thickness of the order of 50 angstrom. A first order expression for R_{sp}, based on the assumption of uniform doping in the source (drain) region, is given by:

$$R_{sp} = \frac{2P_s x X_s}{\pi W} x \ln(\frac{x_j}{t_{ac}} x H) \qquad 3.12$$

Where t_{ac} is the thickness of the surface accumulation layer of length l_{ac} in the gate to source /drain overlap region and H is a factor that has been found to have a value in

the range 0.37-0.9. Note that R_{sh} and R_{sp} are invariant with scaling mainly due to increased P_s.

3.6 Thermal MOSFET models

3.6.1 Noise of a Resistor

Noise is whatever that corrupts the desired signal. One type of noise, is the inductive and capacitive interferences created by the interconnect network may be called external noise. This kind of noise is significant but can be reduced in principle by careful shielding and isolation by circuit designers. The other noise category is called device noise that is inherent to the electronic devices. This kind of noise is due to the random behaviors of the electric carriers inside the device that create voltage and current fluctuations measurable at the terminals of the device.

If a resistor is connected to the input of an oscilloscope, the noise voltage across the resistor is observed. The origin of this noise is the random thermal motion of the charge carriers, and the noise is called the thermal noise. This noise contains many frequency components. If one inserts a frequency filter with band width, Δf and measures the root mean square value of the noise in this frequency band, the results are (Cheng *et al*, 1996)

$$V_n^2 = 4kT\Delta fR$$

3.13

$$I_n^2 = \frac{4kT\Delta f}{R}$$

3.14

Where R is resistance, while I_n^2 presents the noise current that would flow if the resistors terminals were short-circuited. The noise is proportional to Δf but is independent of f. This characteristic is called white noise. The intrinsic thermal noise of MOSFETs originates from the channel resistance.

The channel may be divided into many segments and contributes some noise. The channel noise voltage can be expressed by Equation 3.13 above expressing V_n^2. However, there are several theories of what value should be assigned to R. A classical and popular theory interprets it as $\frac{dV_{ds}}{dI_{ds}}$, or $\frac{1}{g_{ds}}$ in the linear (small V_{ds}) region as given by

$$V_{ds}^2 = \frac{4\gamma kT\Delta f}{g_{ds}}$$

3.14

$$I_{ds}^2 = 4\gamma kTg_{ds}\Delta f$$

3.15

γ is a function of V_{ds} and V_{gs}. At $V_{ds} > V_{sat}$, γ saturates at 2/3, while this model works well at long ó channel length, it underestimates the noise in short-channel MOSFET. In circuit design practice, γ is chosen to fit noise measurements to improve the accuracy of the noise model.

The channel noise voltage also induces a gate current through the gate capacitance. As a result, a portion of the channel noise current flows into the gate network. The gate noise current multiplied by the impedance of the gate input network and the transconductance produces a second noise current at the output. The complete model of the MOSFET noise therefore includes a partially correlated noise source appearing at the gate terminal. This effect can be approximately modeled by lumping the channel voltage at the source.

3.6.2 Current Noise

Detailed and intensive study has been made on different MOSFET device parameters and device behaviours and the temperature dependent terms obtained. Changes in material properties with temperature as well as the contribution to the output current due to the physical structure of MOSFET have been taken into consideration. The temperature dependent compensating currents elements are considered to be in parallel with the MOSFET channel between the drain and the source. These currents

contribute to the total current at high temperature. The three compensating current elements are (Hasanuzzaman *et al*, 2004)

- The body leakage current I_R
- Current change due to the threshold voltage change (I_{TH})
- Current change due to the change of drain and source contact region resistance I_{RDS}.

MOSFET channel current, I_D has been calculated at room temperature using

$$I_D = \frac{W}{L}\mu_n C_{ox}\left(V_{GS} - V_{TH}\right) - V_{DS}/2)V_{DS} \quad 3.16$$

And

$$I_{Dsat} = \frac{W}{2L}\mu_n C_{ox}\left(V_{GS} - V_{TH}\right)^2 \quad 3.17$$

Equation 3.16 is used in the linear region operation and 3.17 is used in the saturation region of the MOSFET. The total drain current can be expressed as

$$I_{total} = I_D + I_R + I_{TH} + I_{RDS} \quad 3.18$$

Where

$$I_R = qA\frac{D_n n_i^2}{L_n N_A} \quad \alpha A T^3 \exp(\frac{-E_g}{kT}) \quad 3.19$$

At room temperature I_R is negligible, I_{TH} and I_{RDS} become zero. However, with increase in temperature, compensating terms contribute to the total current.

Body leakage current is proportional to intrinsic carrier concentration, n_i. At room temperature, n_i of Silicon and Silicon carbide is very low. Thus the contribution of the leakage current is negligible. However, with the increase in temperature, n_i

increases exponentially. Therefore, leakage current contributes to the total current at high temperature. For an n-channel MOSFET device, the temperature dependence of the leakage current can be expressed by Equation 3.19. The 1/T inside the exponent bracket is the dominant temperature factor compared to the T^3 outside the bracket, q is electron charge; A is area of the pn junction and $\propto$ is the proportionality factor.

3.6.3 Threshold voltage

Threshold voltage is the most significant parameter in the study of temperature dependence of MOSFET characteristics. MOSFET current-voltage characteristics are proportional to the square of the difference of gate voltage and threshold voltage. Thus a small change in threshold voltage causes a large change in the output current. Therefore, it is very important to calculate the threshold voltage accurately with temperature changes. Threshold voltage of MOSFET can be deduced using Equation (3.20) (Hasanuzzaman *et al*, 2004)

$$V_{TH} = V_{THO} - \frac{\Delta Q_{it}}{C_{ox}} \pm 2\phi_f \pm \sqrt{2V_{ov}(2|\phi_f|)}$$

3.20

Where is the threshold when the source and substrate are at the same voltage

ΔQ_{it} Is the charge trapped in interface state,

V_{ov} Is overdrive voltage,

and $Ø_f$ is the surface potential given by

$$\phi_f = \frac{kT}{q} \ln\left(\frac{n}{n_i}\right)$$

3.21

The variation of intrinsic carrier concentrations, n_i with temperatures is given by,

$$n_i = (N_c N_v)^2 \exp\left(\frac{-E_g}{2kT}\right)$$

3.22

Where E_g is the band energy

The density of states in the conduction band is n_i and in the valence band is n_v and the band gap energy, E_g can be obtained by (Rosenberg, 1995; Sze and Kwok, 2006; Ytterdal, 1993)

$$N_c \cong 1.73x10^{16} T^{\frac{3}{2}}$$

3.23

$$N_v \cong 4.8x10^{15} T^{\frac{3}{2}}$$

3.24

and

$$E_g \cong E_g(0) - 6.5x10^{-4} x \frac{T^2}{T + 200}$$

3.25

3.6.4 Mobility

Electrons and holes mobilities in a doped semiconductor decreases due to the increase of phonon effects with the temperature. The inversion layer mobility of SiC is much smaller than the bulk mobility. High interface state density plays an important role in inversion layer mobility. Mobilities increases at high temperature where lattice scattering dominates and begins to increase the interface trap charges.

CHAPTER FOUR

METHODOLOGY

4.1 Introduction

This chapter gives a description of the procedure and technique used to carry out a statistical study analysis and drawing of relevant conclusion in this work.

4.2 Statistical Models

4.2.1 Temperature and Velocity

The objective of this research was to investigate temperature effect on the 30nm MOSFET device technology by simulation. This was achieved by modeling an enhancement mode MOSFET.

For operations at the threshold voltages, Equation 4.1 below represents the input and output parameters. In weak inversion the current varies exponentially with gate-to-source bias V_{GS} as given approximately by:

$$I_D = I_{DO} e^{(V_{GS} - V_{th}) / nV_T} \tag{4.1}$$

Where I_{D0} is current at $V_{GS}=V_{th}$, the thermal voltage $V_T=kT/q$ and the slope factor n is given by;

$$n = \left(1 + \frac{C_D}{C_{OX}}\right) \tag{4.2}$$

4.2.2 Saturation or active modes

Modeling for the various modes of MOSFET operations are achieved by using the three formulae representing the various regions:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right) \tag{4.3}$$

$$g_m = \frac{2I_D}{V_{GS} - V_{th}} = \frac{2I_D}{V_{ov}} \tag{4.4}$$

$$\frac{g_m}{I_D} = \frac{1}{nV_T} \qquad 4.5$$

This gives a relationship between transconductance and temperature. The results achieved by this modeling, will correlate with the experimental values for BSIM3v3 (Cheng *et al*, 1997).

4.2.3 Mobility Models

In the modeling, the overall mobility formula is

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_1}\left(\frac{10^6}{E_{eff}}\right)^{\alpha 1} + \frac{1}{\mu_2}\left(\frac{10^6}{E_{eff}}\right)^{\alpha 2} + \frac{1}{\mu_3}\left(\frac{10^{18}}{N_B + \frac{Q_f}{2}}\right)^{-1}\left(\frac{10^{12}}{Q_{inv}}\right)^3 \qquad 4.6$$

Where μ_{eff} is effective mobility, $\mu_{1,}$ $\mu_{2,}$ and μ_3 are mobilities for lateral voltages respectively(Arora,2007).

4.2.4 Mobility Degradation due to Gate Voltage

The effective field has been reported to vary directly with the gate voltage as below.

$$\varepsilon = \frac{C_{ox}}{2\varepsilon_0\varepsilon_{si}}\left(V_{gs} - V_{th} + 2\gamma\sqrt{2\phi_f + V_{sb} - 0.5V_{ds}(2-\alpha)}\right) \qquad \text{(Arora, 2007)} \quad 4.7$$

It can then be clearly seen that gate voltage plays a significant role on the mobility. Higher gate source voltage degrades the mobility as per Equation 4.7. The SPICE MOSFET level 2 model uses the following equation fitted from experimental data.

$$\mu_s = \mu_0\left(\frac{\varepsilon_0\varepsilon_{si}\varepsilon}{C_{ox}(V_{gs} - V_{th} - U_t V_{ds}}\right) \qquad 4.8$$

4.2.5 Carrier Mobility Dependence on Temperature

Carrier mobility exhibits a strong and somewhat complex dependence on temperature. This is because the scattering mechanisms are temperature dependent. For design and

analysis purposes, the dependence of mobility on temperature and dopant concentration are described fairly accurately by the following equations (Arora, 2007)

$$\mu_n = 88T_n^{-0.5} + \frac{7.4x10^3 xT^{-2.33}}{1+((\frac{N}{2.35x10^{17}})T_n^{2.4})^{\alpha}} \qquad 4.9$$

$$\mu_P = 54.3T_n^{-0.57} + \frac{1.36x10^3 xT^{-2.23}}{1+(\frac{N}{(2.35x10^{17})T_n^{2.4}})^{\alpha}}$$

4.10

Where $\alpha = 0.88T_n^{-0.146}$ and $T_n = \frac{T}{300}$

T being measured in Kelvin and N is the total dopant density (cm^{-3}) in the silicon.

4.3 Software Application

The following two softwares were used extensively in this research: MATHCAD and KaleodographÎ for generating graphics and excel for extracting the results from MATHCAD

4.4 MATHCAD

MATHCAD was chosen for the purpose of simulating the characteristics of the MOSFETs because of its easy interface, simple functionality and its ability to export results to excel and being able to draw graphs.

CHAPTER FIVE

RESULTS AND DISCUSSIONS

5.1 Introduction

MOSFETs are not perfect devices and neither are they indestructible and the circuit designer should be aware of the following thermal considerations when designing a system employing MOSFET devices:

Even when fully turned on, a MOSFET will dissipate power ($I^2 R_{DSO}$) due to drain resistance R_{DSO} losses because of the device on-state resistance). This resistance R_{DSO} may cause excessive device temperature which may damage it

Thermal aspects are an important concern when designing power MOSFETs especially in applications which may be operating at elevated ambient temperatures, as the MOSFET junction temperature (T_j) must be kept below 175^0C if operation is to remain within specification.

5.2.1 Drain Current

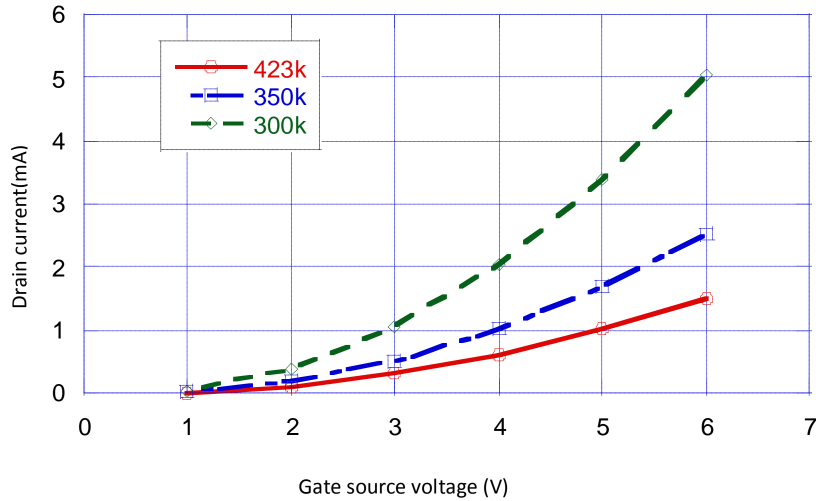


Fig. 5.1: A graph of drain current as a function of gate source voltage.

Figure 5.1 shows the V_{gs}-I_d characteristics at various temperatures. The drain current decreases as the temperature increases. This occurs in the saturated region and is explained by the decrease in mobility with rising temperature. This happens because in the subthreshold region, the subthreshold coefficient is proportional to the temperature. The graph also illustrates nonlinear increasing drain current with increasing gate source voltage. This is explained by the basic threshold model. According to the basic threshold model, the transistor is turned off in the subthreshold region, and there is no conduction between drain and source. In reality, the Boltzmann distribution of electron energies allows some of the more energetic electrons at the source to enter the channel and flow to the drain, resulting in a subthreshold current that is an exponential function of gateósource voltage. While the current between drain and source should ideally be zero when the transistor is being used as a turned-off switch, there is a weak-inversion current, sometimes called subthreshold leakage. This observation leads us to the analysis of mobility effects. At low temperatures only phonon scattering is significant and carriers drift speed is high. The on resistance

decreases as temperature decreases because mobility increases as temperature decreases, and consequently the current increases as shown in the Figure 5.1

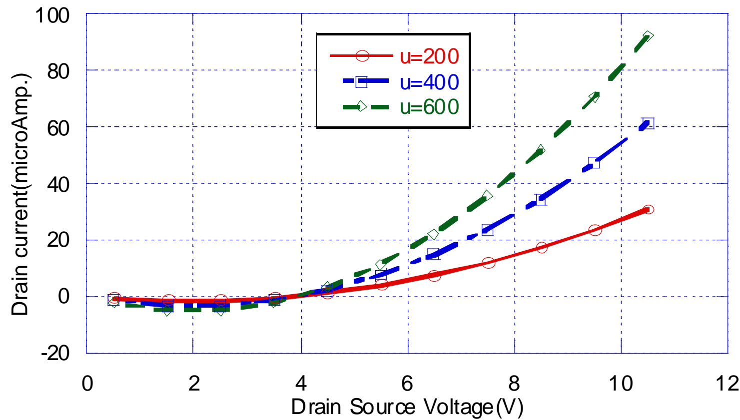


Fig. 5.2: Drain current as a function of the drain source voltage.

For a given mobility, μ say 600 cm^2/V.s, the drain current increases with increasing drain source voltage. This is explained by many electrons being induced at the source for low values of the drain source voltage. Although this work predicts continuous increase in drain current, this may not be accurate. The reason being drain current results from carriers mobility and at certain values of drain source voltage the carriers attain maximum drift velocity and the current curve must flatten.

Considering the mobility value 600 cm^2/V.s, and with working in the weak-inversion region though, the MOSFETs in this region deliver the highest possible transconductance-to-current ratio, namely: $g_m/I_D = 1 / (nV_T)$ almost that of a bipolar transistor as can be seen in Figure 5.3

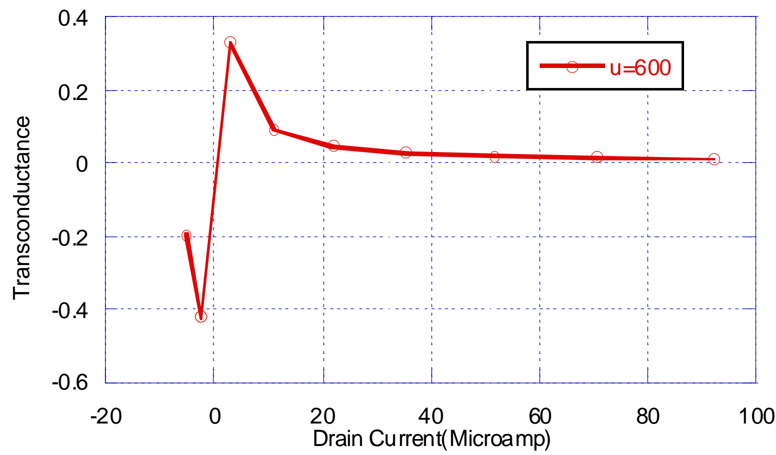


Fig.5.3: A graph of transconductance to current ratio

At low temperatures, for the same transistor under the same bias conditions, higher mobility and transconductance are expected owing to reduced scattering mechanisms.

Considering the mobility value 600 $cm^2/V.s$, and with working in the weak-inversion region, the MOSFETs deliver the highest possible transconductance-to-current ratio, namely: $g_m/I_D = 1 / (nV_T)$,

5.2.2 Drain Source current

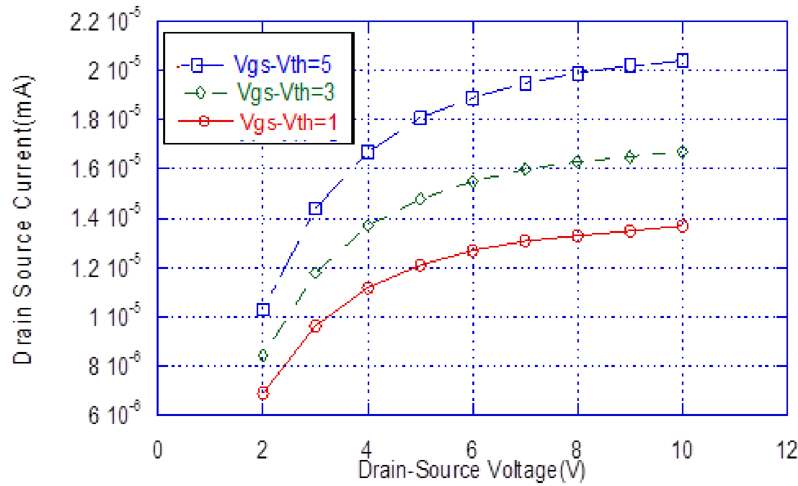


Fig. 5.4: The drain source current verses the drain source voltage.

In the Figure 5.4 there are three different voltage regimes of drain-source voltage.

Considering first case above, when V_{ds} with very small gate source voltage, Vgs = 0, there is little or no drain current (drain source current tends to zero) flowing. This is due to two $n^{+}pn^{+}$ junctions, which are two back-to-back diodes, one of which will be in reverse direction and therefore block the current flow. This is the depletion mode of operation. Holes in semiconductor are repelled by positive charge on the gate. The semiconductor is depleted of free holes and a depletion layer is created. When $V_{gs} > 0$, a strongly positive gate voltage results. This becomes the inversion mode of operation. Electrons are induced in the semiconductor near the oxide-semiconductor interface. An electron current flows from source to drain. The magnitude of the gate voltage determines the magnitude of the SD current.

In the second case, the drain current rises rapidly, because a small drain-source voltage slightly greater than zero ($V_{DS} > 0$) and $V_{GS} >> 0$, (inversion mode) is present, the electric field in the oxide field is higher at the source end of the channel and is lower at the drain end of the channel. Thus many electrons are induced near the source and few electrons are induced near the drain. An increasing drain source

voltage has two effects (i) I_{DS} increases and (ii) fewer electrons at the drain end of the channel.

For very large drain-source voltage (V_{DS}>> 0), and V_{GS}>> 0, the curve flattens i.e. the drain source current saturates; still we have the inversion mode. Electric field in the oxide is highest at the source end of the channel. There are many electrons near source. At the drain end of the channel electric field is zero or lowest. Therefore no free electrons are present near drain. The curve flattens and channel is pinched off. It is worth noting also that for large drain source voltage, the carriers reach their maximum drift velocity and the current amplitude cannot increase.

5.2.3 Self heating

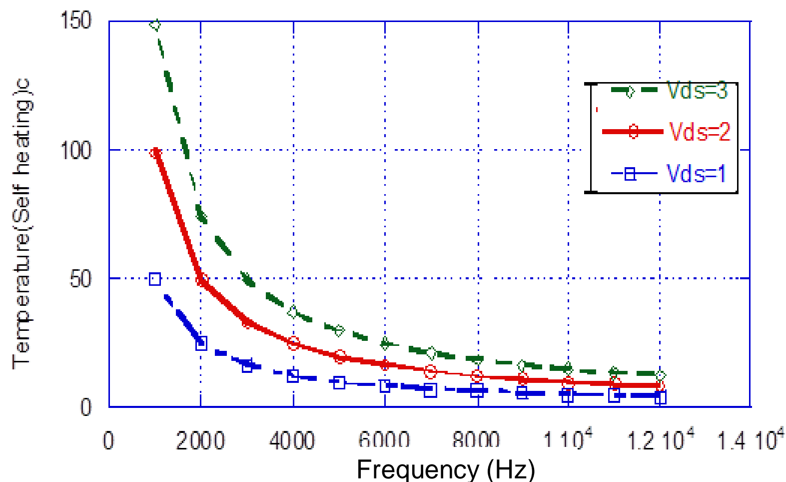


Fig.5.5: Graph of temperature as a function of frequency.

Higher frequency operations require lower temperatures and consequently higher efficiency of MOSFET.

In Figure 5.5 the frequency values increase with temperature decrease. The low lattice temperature in the MOSFET film increases mobility and saturation velocity of carriers, while at the same time minimizing carrier scattering. Low temperatures also favour faster relaxation time and minority carrier diffusions from source to drain. The high mobility leads to a higher current, transconductance and transition frequency.

However, at higher temperatures, stresses results in the drain region, drain current reduces resulting into device degradation evidence by low frequency operations and speeds.

5.3 Challenges With Chip Reduction

As MOSFETs become smaller, the number of atoms in the silicon that produce many of the transistor's properties is becoming fewer. This results in control of dopant numbers being more erratic. The transistor characteristics become less certain, more statistical.

5.3.1 Threshold Voltage at Different Device Sizes

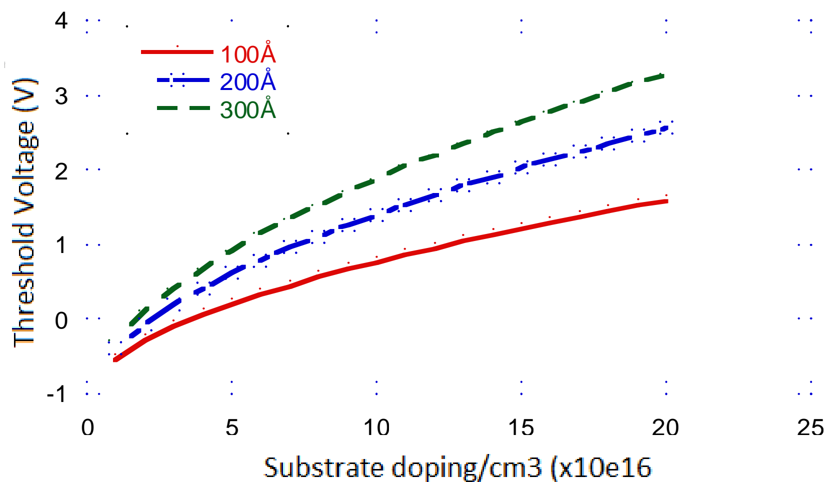


Fig. 5.6: Substrate doping concentrations effects on threshold voltage.

Higher doping requires higher threshold voltage to turn on the MOSFET as can be seen from the Figure 5.6 above. In the Figure, the threshold voltage as a function of doping concentration is presented. The threshold voltage is the minimum gate voltage that initiates drain current flow. While a high value of threshold V_{gs} can apparently lengthen turn ON delay time, a low value for power MOSFET is undesirable because the high gate impedance of a MOSFET makes it susceptible to spurious turn-on due to gate noise.

Low threshold V_{gs} requires thinner oxides, which lowers the gate oxide voltage rating. Threshold voltage increases with substrate doping because the thickness increases, thereby increasing carrier concentration. The threshold voltage also increases as temperature is reduced because of reduction in phonon scattering. The increase in threshold voltage results in reduction of the overdrive voltage and a drop in current while constant, g_m biasing is used.

As MOSFET geometries shrink, the voltage that can be applied to the gate must be reduced to maintain reliability. To maintain performance, the threshold voltage of the MOSFET has to be reduced as well. As threshold voltage is reduced, the transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available; the circuit design is a compromise between strong current in the ON case and low current in the OFF case, and the application determines whether to favor one over the other.

5.4.1 Effective Carrier Mobility

In Figure 5.7 below the effective mobility model is presented. The curves are drawn at different values of the gate voltage. It shows that the effective mobility show little variation with effective transverse field for a given value of gate voltage say 6V as seen in the Figure 5.7 This is because an increase in effective field causes carriers to be drawn closer to the interface, thus increasing surface scattering and hence reduce mobility. On the other hand, the Figure shows that mobility for gate voltage equal to 6V is less than gate voltage equal to 4V. This is due to the limiting coulomb scattering mechanism resulting from interface states and fixed oxide charges being dominant. Also, when carriers are accelerated in an electric field their velocity will begin to saturate at high enough electric fields. This effect has to be accounted for by a reduction of the effective mobility. The mobility thus degrades with increasing gate voltage.

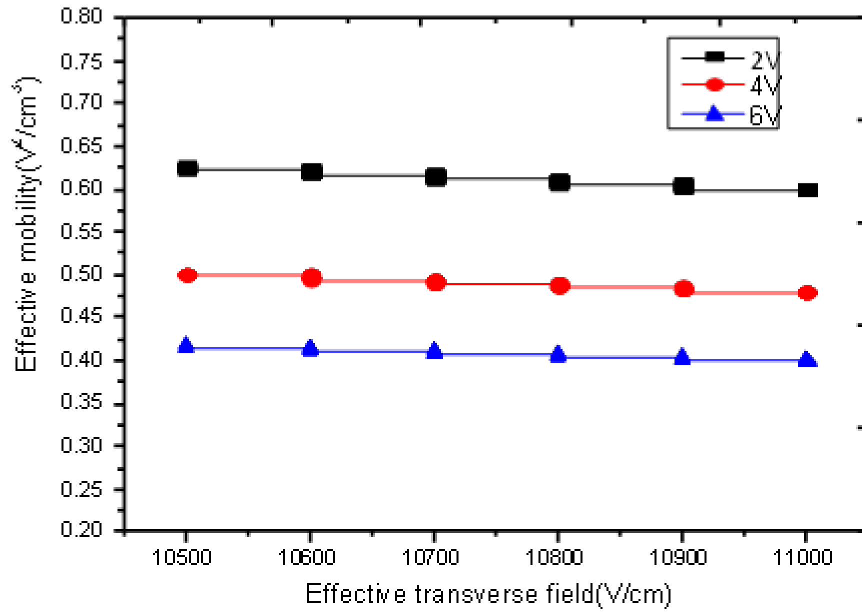


Fig 5.7: Effective mobility as a function of electric field.

In Figure 5.8 carrier mobility effects as a function of overall effective field is presented. The mobility decreases as is the case in Figure 5.7. However, in Figure 5.8, there is very little variance with different sizes of the oxide thickness. Under electric fields, the carrier undergo increased scattering with increasing fields.

This happens because the normal field ε_x acts in a direction so as to accelerate the charge carriers towards the surface causing the carriers to scatter more frequently than in the absence of the gate field. On the other hand, the lateral field ε_y causes charge carriers to move faster, so that at high enough V_{ds}, the carriers become velocity saturated.

5.4.2 Carrier mobility

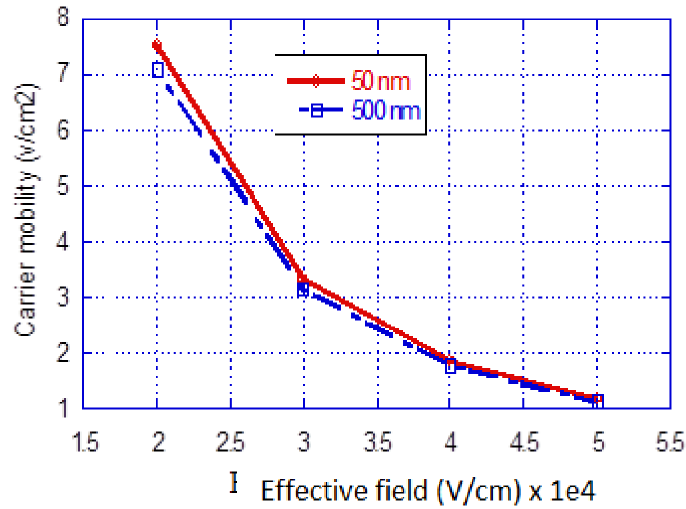


Fig. 5.8: Illustration of carrier mobility as a function of effective field.

The thin-oxide MOSFET transconductance is degraded by the finite inversion layer capacitance and not by decreased mobility for thin oxides.

However, dependence of mobility on oxide thickness can be observed for thickness lower than 100Å, in some cases (Arora, 2007). In comparison of this observation to the above analysis, it can be comfortably concluded that mobility is more a function of other factors like Si-SiO_2 interface than the device parameters such as oxide thickness or doping concentration.

5.4.3 Carrier Mobility and Effective Field

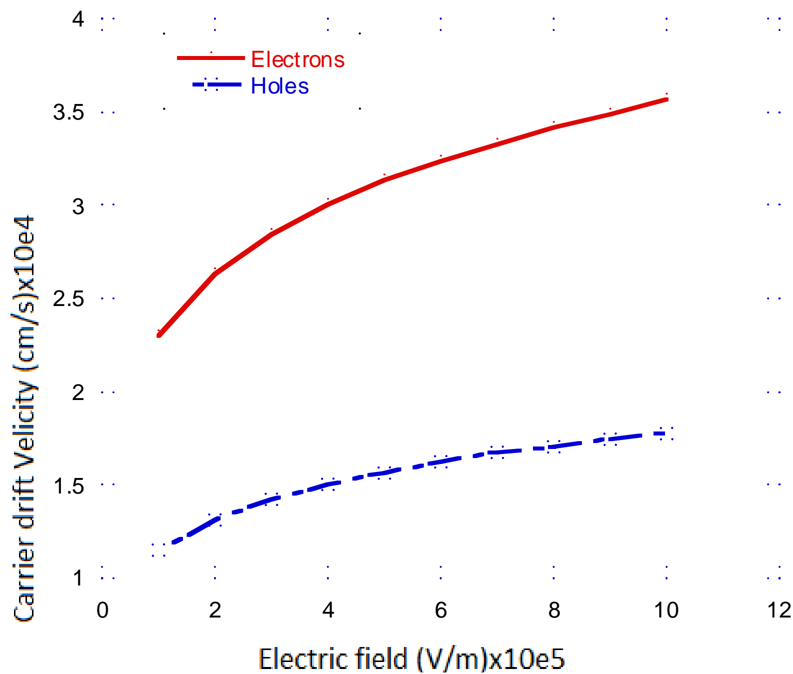


Fig. 5.9: A graph of carrier drift velocity as a function of electric field for both electrons and holes.

In Figure 5.9 the carrier drift velocity for electrons and holes is shown. It is very clear for same range of electric field; the electron drift velocity is higher than that of Holes.

This is attributed to scattering that affects Holes more than electrons. It can also be attributed to the fact that electrons have less mass compared to Holes and hence the drift velocity for electron would always be higher than the one for Holes for a given electric field

5.5 Carrier Mobility Dependence on Temperature

Carrier mobility exhibits a strong and somewhat complex dependence on temperature. This is because the scattering mechanisms are temperature dependent.

Equation 4.9 and 4.10 illustrates the dependence of mobility on temperature. In Figures 5.10 and Figure 5.11, the temperature dependence on temperature is presented.

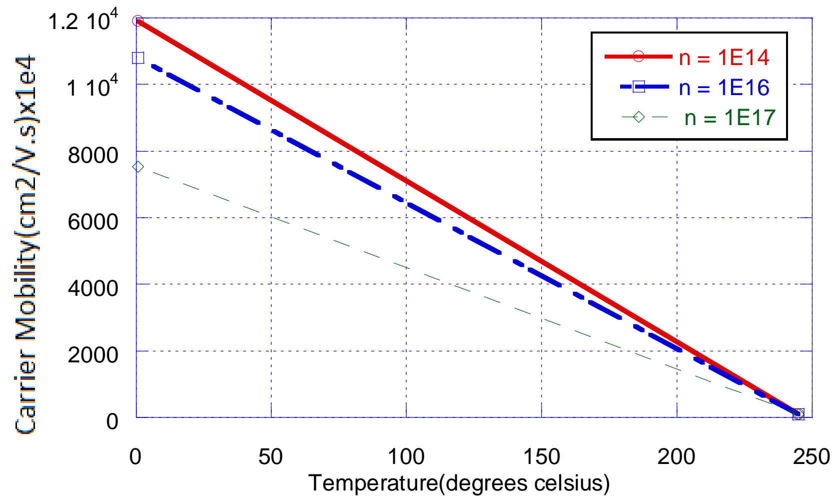


Fig 5.10: Carrier mobility as a function of temperature for different carrier concentrations.

Figure 5.10 show carrier mobility decreasing with higher carrier concentrations. For different carrier concentration, temperature lowers the mobility. At low temperatures, mobility is largely dependent on carrier concentration. But as the temperature increases, mobility is significantly affected by scattering caused by high phonon concentration

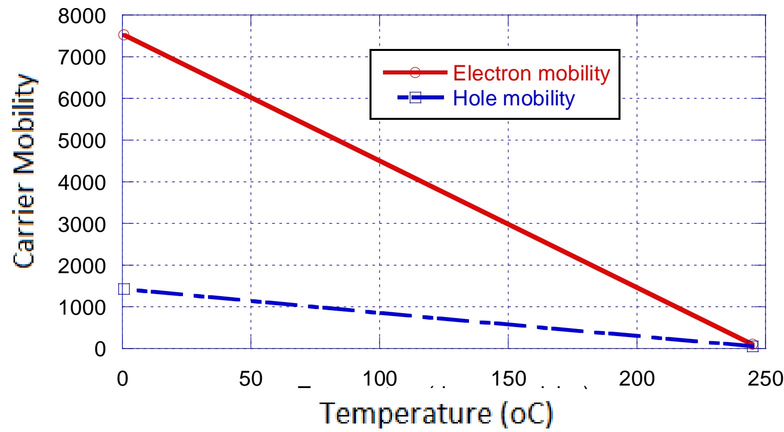


Figure 5.11: Carrier mobility as a function of temperature for hole and electron.

Figure 5.11 shows that carrier mobility for electrons is higher than that of Holes. As has been previously discussed many factors come into play at higher temperatures. For example scattering mechanisms like impurity scattering, ion centers, defect centers etc. become dominant at higher temperatures. Anharmonic terms equally set in. High carrier concentration may make the channel and oxide õmetallicö. All these impede charge flow at high temperatures.

5.6 Sheet Resistance

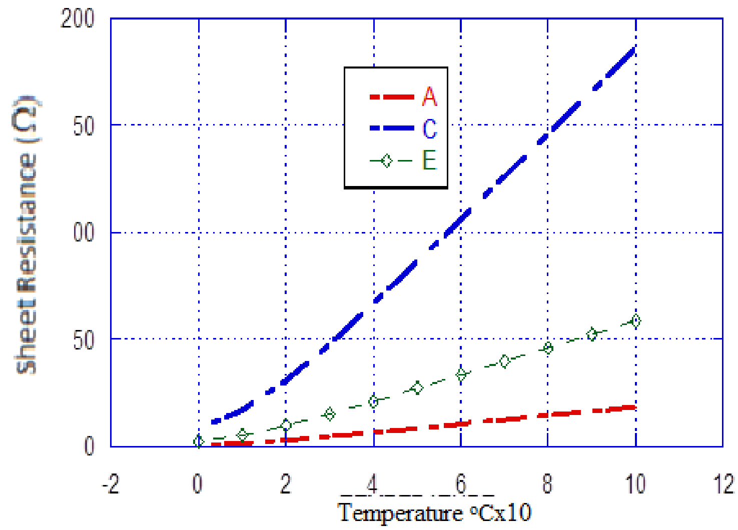


Fig 5.12: A graph of MOSFET film resistance as a function of temperature.

The impact of the total resistance on MOSFET scaling is significant. The results in Figure 5.12 shows a relationship between sheet resistance and temperature. In these findings, the sheet resistance increases with temperature. This possibly due to decreased mobility and inclusion of the metallic contact. Degradation in speed due to series resistance in the short channel MOSFET is a factor contributing to the observed results.

5.7 Device speed

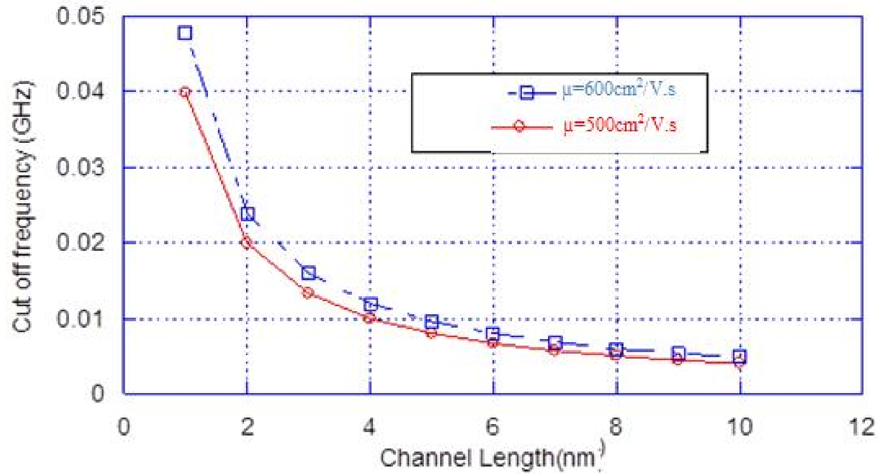


Fig.5.13: A graph of cut off frequency as a function of channel length.

In Figure 5.13, the cut off frequency as a function of channel length at various mobility values is presented. The decrease in cut off frequency as channel length increases is attributed to increase in gate capacitance resulting from the increasing channel length. The gate overlap capacitances and the extrinsic capacitances retard switching speeds. However, the cut off frequency show no much dependence on mobility as shown by the two curves.

CHAPTER SIX

CONCLUSION AND RECOMMENDATIONS

6.1 Conclusions

In this work, the effect of temperature on the metal oxide field effect transistor MOSFET has been investigated. The following results were obtained.

The drain current reduces with decreasing mobility and gate source voltage. However the drain current increases with reducing temperature. This happens majorly in the saturated region. At low temperatures only phonon scattering is significant. The other scattering mechanisms like ion scattering are very minimal (however they are dominant at high temperatures). Therefore carriers drift speed is very high. This consequently reduces the ON resistance. On the other hand, as temperature decreases mobility increases. This too reduces the on resistance and consequently the current increases.
High frequency operations occur at lower temperatures. This is quite visible in Figure 5.5. The low lattice temperature in MOSFET film increase mobility and saturation velocity of carriers. This high mobility leads to a higher current, transconductance and transition frequency.

As MOSFET device size becomes smaller by the day, random process variations affect all dimensions i.e. oxide thickness, junction depths, channel lengths etc. The results show that the transistor characteristics become less certain, more statistical. In Figure 5.6 threshold voltage increases with substrate doping. Comparing for a substrate doping concentration of $10^{16}/cm^3$, thickness of $100\overset{o}{A}$ gives a lesser threshold voltage as compared to that of 300 $\overset{o}{A}$ and for a particular value of doping concentration reduces with thickness. From this model it is very clear therefore that fabrication variation complicates optimization for performance of this device. It therefore means designers have to be aware of the limitation of scaling down of MOSFETs.

Scaling intend to minimize device size and consequently the cost of silicon used. When device size becomes small effects of capacitance becomes small. The smaller a device is the less is its threshold voltage and the more it becomes vulnerable to even smaller temperature changes.

6.2 Recommendations

In the process of the investigations, a number of issues came up that could help shade more light on the studied process. Some of the areas were:

1. Need for thorough optimization of deposition conditions.
2. Studies on the temperature dependence of substrate capacitance.

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